REMARKS

Claims 1-21 and 23-29 are currently pending in the subject application, and are presently under consideration. Claims 27-29 have been allowed. Claims 4, 5, 8-10, 13, 14, 16-19 and 24-26 have been indicated as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 18 and 19 have been amended to correct typographical errors. Claims 1-3, 6, 7, 11, 12, 15, 20, 21 and 23 stand rejected.

Favorable reconsideration of the application is requested in view of the amendments and comments herein.

I. Rejection of Claims 1 and 23 Under 35 U.S.C. §102(b)

Claims 1 and 23 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,362,755 to Tinker ("Tinker"). Withdrawal of this rejection is respectfully requested for at least the following reasons.

The Office Action contends that claim 1 is anticipated by Tinker by referring to Col. 6, Fig. 7 and to claim 13 of Tinker. However, a thorough reading of Tinker as a whole reveals several deficiencies of Tinker relative to the claim 1. For instance, Tinker discloses at Col. 6, lines 32-40 that the look up table provides two outputs, namely a corresponding integrated sample and a maximum integrated sample based on the address and the input sample data. The multiplexer 78 then selects one of these two outputs depending whether the state of the input data sample changes. In sharp contrast, the aggregator of claim 1 aggregates the output samples to provide an aggregated output stream signal. The function performed by the aggregator (*i.e.*, aggregating the output samples to provide the output stream signal) is substantially different from the selection of one of the output signals, as taught by the multiplexer of Tinker. Additionally, claim 1 recites that the desired output sample rate is different from the input sample rate according to the first sample rate 52, which is based on the first clock signal 88 (Tinker at Col. 6, lines 15-16). Applicant submits that Tinker teaches that the address 84 and the

output of the multiplexer would be at the same sample rate. That is, Tinker fails to teach or suggest that the output of the multiplexer 78 would be at a different sample rate from the address 84, as recited in claim 1. For these reasons, claim 1 is not anticipated by Tinker.

With regard to claim 23, the Office Action fails to provide evidence that Tinker teaches means for storing look up table data that represents delta sigma modulated outputs, as recited in claim 23. Based on a complete review of Tinker, Applicant submits that this failure is because Tinker does not contain such a teaching. Instead, Tinker discloses that the look-up table stores predetermined integrated samples that are indexed according to different addresses produced by an addressing module 74 (See Tinker, Col. 6, lines 22-40). Specifically, the look-up table 76 is programmed with the predetermined integrated samples, such as according to the description provided with respect to Figs. 2-6 of Tinker (See Tinker, Col. 6, lines 31-40). Accordingly, for these reasons as well as for reasons similar to those stated above with regard to claim 1, claim 23 is not anticipated by Tinker.

Accordingly, reconsideration and allowance of claims 1 and 23 are respectfully requested.

II. Rejection of Claims 2-3, 6-7, 11-12, 15 and 20-21 Under 35 U.S.C. §103(a)

Claims 2-3, 6-7, 11-12, 15 and 20-21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tinker as applied to claim 1 above, and further in view of U.S. Patent No. 6,489,908 to Panasik, et al. ("Panasik"). Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claims 2-3, 6-7 and 11-12 are allowable for at least the same reasons as claim 1 discussed above.

Regarding claim 2, the Office Action cites Panasik for a purported teaching of a memory system that provides N output samples that represent delta-sigma modulated data. The Office Action then concludes that it would have been obvious to incorporate Panasik's circuit in to

Tinker's circuit to improve sampling conversion. Applicant respectfully traverses this conclusion.

The combined teachings of Tinker and Panasik, as suggested in the Office Action fails to render either of claims 2 or 3 obvious. For instance, if the read-only memory 110 of Panasik were incorporated into Tinker, as suggested in the Office Action, Applicant submits that there is no evidence to support that sampling conversion would be improved. In sharp contrast, an inoperable system would likely result. For example, since the look-up table 76 of Tinker is configured to output predetermined integrated samples based on a generated address 84, the use of Panasik's read-only memory 110 would provide sigma-delta converted outputs. That is, since the read-only memory 110 of Panasik is substantially different in function and result from the look-up table 76 of Tinker, there is nothing in the prior art to suggest that the read-only memory 110 of Panasik would function properly if incorporated into the sample module 44 of Tinker. Accordingly, in further contrast to the contention in the Office Action, there is not proper motivation for the combination; namely, "to incorporate Panasik's circuit into Tinker's circuit," as stated in the Office Action. The purported improvement in sampling conversion thus appears to be based on a subjective belief or hindsight by the Examiner, which is improper. See *In re Lee*, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir 2002). Reconsideration and allowance of claim 2 is respectfully requested. In the absence of allowance of claim 2, Applicant respectfully requests that the Office present evidence of a suggestion or motivation for one of skill in the art to combine prior art references to produce system of claim 2.

With regard to claim 3, as mentioned above, Tinker fails to teach or suggest that the look-up table 76 would operate at a rate that is less than the output rate of the multiplexer 78. The change in sample rate (or rate conversion) in Tinker results from the subsequent integration and differentiation performed by modules 46 and 48 (See Tinker at , referring back to Col. 5, line 63, through Col. 6, line 9). Thus, allowance of claim 3 is respectfully requested.

With regard to claim 11, the Office Action cites Panasik for its teaching of a plurality of digital to analog converters and contends that it would have obvious to incorporate Panasik's circuit into Tinker's circuitry to improve sampling conversion. Firstly, how would use of any DACs, as taught by Panasik, improve sampling conversion, especially since the sampling conversion occurs solely in the digital domain?

Additionally, Panasik discloses that a plurality of digital-to-analog converters 120, 122, 124, 126 are utilized in parallel and that the separate (or non-aggregated) signals from each of the plurality of DACs are obtained by clocking each of the DACs with the delayed multi phase clock signal. Panasik fails to teach a digital-to-analog converter that converts the aggregated output stream signal to a corresponding analog signal having a center frequency functionally regulated to the desired output sample rate. Instead, as mentioned above, each of the one bit DACs 120, 122, 124 and 126 is clocked at a different time period by the multi phase clocks to provide the corresponding output signal. For these reasons, reconsideration of claim 11 is respectfully requested.

Claim 12 depends from claim 11 and further recites an antenna that is operative to propagate a wireless signal at a transmission frequency based on the corresponding analog signal. Since claim 12 depends from claim 11 it is allowable for at least substantially the same reasons as claim 11.

Claim 15 is allowable for similar reasons to those stated above with respect to claims 1, and 11. In brief, claim 15 recites that the look-up table provides a set of digital output samples at a sample rate that is different from the sample rate of the input sample. In contrast, the look-up table of Tinker 76 provides the output signal at the same rate as the input sample; namely, according to the first sample rate 52. Additionally, as presented above with respect to claim 2, there is not proper motivation to combine Panasik and Tinker. Therefore, reconsideration and allowance of claim 15 are respectfully requested.

Claims 20 and 21 are further allowable for the same reasons that claim 15 is allowable.

For the reasons described above, claims 2-3, 6-7, 11-12, 15 and 20-21 should be patentable over the cited art. Accordingly, withdrawal of this rejection is respectfully requested.

III. Double Patenting

Claims 1-3, 6-7, 11-12, 15, 20-21 and 23 stand rejected under the judicially created doctrine of double patenting over claims 5-31 of U.S. Patent No. 6,873,280. However, a review of claims 5-31 quickly reveals that inappropriateness of the double patenting rejection. The Office Action oversimplifies claims 1-3, 6-7, 11-12, 15, 20-21 and 23 as including the following common subject matter: "a signal conversion system having memory or look up table (18) and output digital signal (20) to an aggregator (10) and dac (26) of Fig. 1 of USP 6.873.280." Significantly, the characterization of claims 1-3, 6-7, 11-12, 15, 20-21 and 23 used to support the double patent rejection, however, is an oversimplification that fails to consider all recitations in claims 1-3, 6-7, 11-12, 15, 20-21 and 23, which would be necessary to support a same invention double patenting rejection.

For instance, claim 5 of U.S. Patent No. 6,873,280 recites:

> A signal conversion system comprising:
>
> a plurality of parallel stages, each of the parallel stages being operative to perform at least one of filtering, noise shaping and quantization on a respective sample of a digital input signal and provide a corresponding output signal at a rate that is functionally related to the number of parallel stages,
>
> each of the parallel stages further comprising a delta-sigma modulator operative to perform the noise shaping and quantization and to provide the corresponding output signal for the respective parallel stage, and
>
> each of the delta-sigma modulators further comprises a complementary metal-oxide semiconductor (CMOS) delta-sigma modulator.

Thus, by way of comparison, claims 1-3, 6-7, 11-12, 15, 20-21 and 23 do not recite the plurality of parallel stages, as recited in claim 5 of U.S. Patent No. 6,873,280. Neither do claims 5-31 recite: "a memory system programmed to provide a set of digital output samples in response to a given digital input sample, each of a plurality of possible input samples being associated with a

corresponding set of plural digital output samples," as recited in claim 1 of the present application. Additional differences between the claimed subject matter become apparent by comparison of various other claims in the instant application relative to claims 5-31 in U.S. Patent No. 6,873,280. Since claims 1-3, 6-7, 11-12, 15, 20-21 and 23 are not coextensive in scope with any of claims 5-31 in U.S. Patent No. 6,873,280, withdrawal of the double patenting rejection is respectfully requested. In the absence of withdrawal of the double patenting rejection, Applicant requests that the Examiner present a detailed comparison of the claims 1-3, 6-7, 11-12, 15, 20-21 and 23 of the instant application relative to claims 5-31 in U.S. Patent No. 6,873,280 sufficient to support this rejection.

IV. Allowable Subject Matter

Claims 4-5, 8-10, 13-14, 16-17, 18-19 and 24-26 are objected to as being dependent upon a rejected base claim, and would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Objected claims recite features that are not taught or suggested in the prior art.

Claims 27-29 have been allowed.

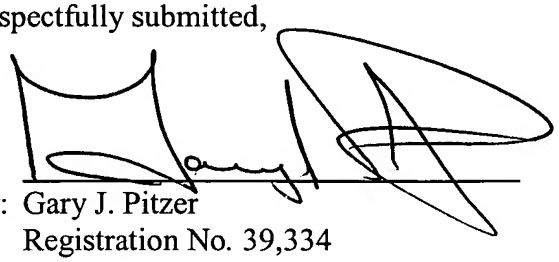
V. CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

If the Examiner has any questions or if the Applicant or its representative can be of any assistance in connection with prosecution of this application, the Examiner is invited and encouraged to contact the undersigned at the number identified below.

Please charge any deficiency or credit any overpayment in the fees for this amendment to our Deposit Account No. 20-0090.

Respectfully submitted,



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